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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,637	06/01/2001	Brian Boles	18153.0033	9037

23517 7590 05/03/2004

SWIDLER BERLIN SHEREFF FRIEDMAN, LLP
3000 K STREET, NW
BOX IP
WASHINGTON, DC 20007

EXAMINER	
O BRIEN, BARRY J	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/03/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,637	BOLES ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/1/01, 9/13/01, 11/16/01, 12/11/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4 and 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-46 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 9/13/01, IDS as received on 11/16/01, and Preliminary Amendment as received on 12/11/01.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claims 2, 4, 6, 10, 13-15, 17, 21, 25, 27, 29, 33, 36-38, 40 and 44 are objected to because of the following informalities:

a. Claims 2, 4, 6, 10, 13-15, 17, 21, 25, 27, 29, 33, 36-38, 40 and 44 recite the limitations "the first memory location" or "the second memory location". There is no antecedent basis for these terms. Please correct the claim language to read

"the first data memory location" and "the second data memory location", respectively, in order to provide the correct antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 4, 8, 12, 19, 23, 27, 31, 35, 42 and 46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 4 recites the limitation, "writing the operand to the first memory location" on its second line. This limitation is unclear in relation to the parent claims of claim 4. Not only does the parent claim of claim 4 recite that the "step of executing the bit value transfer instruction" writes to a location in the second memory specified by said instruction, but there would be no "transfer" taking place if the instruction read data from a memory location and wrote it directly back to the same location. Please correct the claim language to more clearly point out the metes and bounds of the claim. For the purposes of this examination, the examiner will assume that the limitation in the claim writes the operand to the second memory location. See a similar problem in claim 27.

9. Claim 8 recites the limitation, "data memory" on its second line. There is insufficient antecedent basis for this limitation in the claims. Please correct the claim language to more clearly define this term and how it relates to the rest of the claim language. For the purposes of

this examination, the Examiner will assume that, because other claims are directed towards registers being data memory locations, and because there is no claimed "data memory", that the "address in data memory" is the address of a register location. See a similar problem in claims 12, 19, 23, 31, 35, 42 and 46.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-4, 13-15, 24-27 and 36-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Weng et al., U.S. Patent No. 5,765,216.

12. Regarding claim 1, Weng has taught a method of processing a bit transfer operation instruction (see Col.2 lines 37-64), comprising:

a. Fetching and decoding a bit value transfer instruction (see Col.4 lines 13-39),

b. Executing the bit value transfer instruction on a source bit position of a first data memory location to select a bit value in the source bit position of the first data memory location, the bit position of the first data memory location specified in the bit value transfer instruction (see Col.3 lines 34-55 and Col.5 lines 38-58),

c. Writing the value to a destination bit position of a second data memory location, the destination bit position specified in the bit value transfer instruction (see Col.3 lines 34-55 and Col.5 lines 38-58).

13. Regarding claim 2, Weng has taught the method according to claim 1, wherein the step of executing the bit value transfer instruction includes reading an operand at the first memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

14. Regarding claim 3, Weng has taught the method according to claim 2, wherein the step of executing the bit value transfer instruction includes copying the bit value at the source bit position of the operand (see Col.3 lines 34-55 and Col.5 lines 38-58).

15. Regarding claim 4, Weng has taught the method according to claim 3, wherein the step of executing the bit value transfer instruction includes writing the operand to the first memory location (see above paragraph 8, Col.3 lines 34-55 and Col.5 lines 38-58).

16. Regarding claim 13, Weng has taught the method according to claim 1, wherein the step of executing the bit value transfer instruction includes reading an operand at the second memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

17. Regarding claim 14, Weng has taught the method according to claim 13, wherein the step of executing the bit value transfer instruction includes copying the bit value at the source bit position of the first memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

18. Regarding claim 15, Weng has taught the method according to claim 14, wherein the step of executing the bit value transfer instruction includes writing the operand to the second memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

19. Regarding claim 24, Weng has taught a processor for bit transfer operation instruction processing (see Col.2 lines 37-64), comprising:

a. A program memory for storing instructions including a bit value transfer operation instruction. Here, while a program memory has not been explicitly

taught, bit value transfer instructions being input for decoding and execution have been taught (see Col.4 lines 24-39). Thus it is inherent that a program memory exists in order to store the incoming instructions, as the instruction can't all be input to the decoder simultaneously, and require some sort of storage to hold them prior to execution.

b. A program counter (64 of Fig.4) for identifying current instructions for processing (see Col.6 lines 52-64),

c. An arithmetic logic unit (ALU) (45 of Fig.3) for executing instructions within the program memory, the ALU including:

I. Bit value transfer operation logic for executing the bit value transfer operation instruction on a source bit position of a first data memory location to select a bit value in the source bit position of the first data memory location, the bit position of the first data memory location specified in the bit value transfer instruction (see Col.3 lines 34-55 and Col.5 lines 38-58),

II. Writing the value to a destination bit position of a second data memory location, the destination bit position specified in the bit value transfer instruction (see Col.3 lines 34-55 and Col.5 lines 38-58).

20. Regarding claim 25, Weng has taught the processor according to claim 24, wherein the step of executing the bit value transfer instruction includes the ALU reading an operand at the address in the first memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

21. Regarding claim 26, Weng has taught the processor according to claim 25, wherein the step of executing the bit value transfer instruction includes the ALU copying the bit value at the source bit position of the operand (see Col.3 lines 34-55 and Col.5 lines 38-58).

22. Regarding claim 27, Weng has taught the processor according to claim 26, wherein the step of executing the bit value transfer instruction includes the ALU writing the operand to the address in the first memory location (see above paragraph 8, Col.3 lines 34-55 and Col.5 lines 38-58).

23. Regarding claim 36, Weng has taught the processor according to claim 24, wherein the step of executing the bit value transfer instruction includes the ALU reading an operand at the address in the second memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

24. Regarding claim 37, Weng has taught the processor according to claim 36, wherein the step of executing the bit value transfer instruction includes the ALU copying the bit value at the source bit position of the first memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

25. Regarding claim 38, Weng has taught the processor according to claim 37, wherein the step of executing the bit value transfer instruction includes the ALU writing the operand to the address in the second memory location (see Col.3 lines 34-55 and Col.5 lines 38-58).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 5-12, 16-23, 28-35 and 39-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weng et al., U.S. Patent No. 5,765,216, in further view of Gerson et al., U.S. Patent No. 4,451,885.

28. Regarding claims 5 and 28, taking claim 28 as exemplary, Weng has taught the processor according to claim 27, but has not explicitly taught wherein the bit value transfer instruction is a first test bit value transfer instruction.

29. However, Gerson has taught a test bit copy instruction which transfers a test bit value from a memory location to a carry status bit memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26) so that test bit transfers can take place without a branch instruction (see Gerson, Col.1 lines 27-30), thereby improving the speed at which bit operations can take place (see Gerson, Abstract). Because it is desirable to improve the speed of processing all operations, let alone bit operations, one of ordinary skill in the art would have found it obvious to modify the bit value transfer instruction of Weng to be a test bit transfer instruction so that speed of bit processing operations is increased due to bit transfers being allowed to happen without a corresponding branch instruction.

30. Claim 5 is nearly identical to claim 28, differing in its parent claim, but encompassing the same scope as claim 28. Therefore, claim 5 is rejected for the same reasons as claim 28.

31. Regarding claims 6 and 29, taking claim 29 as exemplary, Weng in view of Gerson has taught the processor according to claim 28, wherein the first test bit value transfer instruction specifies a carry status bit position as the destination bit position of the second memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

32. Claim 6 is nearly identical to claim 29, differing in its parent claim, but encompassing the same scope as claim 29. Therefore, claim 6 is rejected for the same reasons as claim 29.

33. Regarding claims 7 and 30, taking claim 30 as exemplary, Weng in view of Gerson has taught the processor according to claim 29, wherein the first test bit value transfer instruction specifies a register as the first data memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

34. Claim 7 is nearly identical to claim 30, differing in its parent claim, but encompassing the same scope as claim 30. Therefore, claim 7 is rejected for the same reasons as claim 30.

35. Regarding claims 8 and 31, taking claim 31 as exemplary, Weng in view of Gerson has taught the processor according to claim 29, wherein the first test bit value transfer instruction specifies an address in data memory as the first data memory location (see above paragraph 9, as well as Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

36. Claim 8 is nearly identical to claim 31, differing in its parent claim, but encompassing the same scope as claim 31. Therefore, claim 8 is rejected for the same reasons as claim 31.

37. Regarding claims 9 and 32, taking claim 32 as exemplary, Weng has taught the processor according to claim 27, but has not explicitly taught wherein the bit value transfer instruction is a second test bit value transfer instruction.

38. However, Gerson has taught a test bit copy instruction which transfers a test bit value from a carry status bit memory location to a memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26) so that test bit transfers can take place without a branch instruction (see Gerson, Col.1 lines 27-30), thereby improving the speed at which bit operations can take place (see Gerson, Abstract). Because it is desirable to improve the speed of processing all operations, let

alone bit operations, one of ordinary skill in the art would have found it obvious to modify the bit value transfer instruction of Weng to be a test bit transfer instruction so that speed of bit processing operations is increased due to bit transfers being allowed to happen without a corresponding branch instruction.

39. Claim 9 is nearly identical to claim 32, differing in its parent claim, but encompassing the same scope as claim 32. Therefore, claim 9 is rejected for the same reasons as claim 32.

40. Regarding claims 10 and 33, taking claim 33 as exemplary, Weng in view of Gerson has taught the processor according to claim 32, but has not explicitly taught wherein the second test bit value transfer instruction specifies a zero status bit position as the destination bit position of the second memory location.

41. However, while the bit transfer operation of Gerson involves transferring a value to and from the carry status bit, Gerson also has taught that any bit, such as an overflow bit, in the status register (Gerson, 28 of Fig.1) could also be used as the bit to be transferred into or from (see Gerson, Col.2 lines 26-34). Official Notice is taken that along with carry and overflow bits, a status register generally has a zero bit representing if a recent comparison had a result with a value of zero. Because Gerson has taught that any status bit can be used as a source and destination of a bit transfer operation, and it is well known that a zero bit is included as a status bit, one of ordinary skill in the art would have found it obvious to include the zero bit in the status register as a possible destination of a bit transfer operation.

42. Claim 10 is nearly identical to claim 33, differing in its parent claim, but encompassing the same scope as claim 33. Therefore, claim 10 is rejected for the same reasons as claim 33.

43. Regarding claims 11 and 34, taking claim 34 as exemplary, Weng in view of Gerson has taught the processor according to claim 33, wherein the second test bit value transfer instruction specifies a register as the first data memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

44. Claim 11 is nearly identical to claim 34, differing in its parent claim, but encompassing the same scope as claim 34. Therefore, claim 11 is rejected for the same reasons as claim 34.

45. Regarding claims 12 and 35, taking claim 35 as exemplary, Weng in view of Gerson has taught the processor according to claim 33, wherein the second test bit value transfer instruction specifies an address in data memory as the first data memory location (see above paragraph 9, as well as Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

46. Regarding claims 16 and 39, taking claim 39 as exemplary, Weng has taught the processor according to claim 38, but has not explicitly taught wherein the bit value transfer instruction is a first write bit value transfer instruction.

47. However, Gerson has taught a test bit copy instruction which transfers a write bit value from a carry status bit memory location to a memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26) so that write bit transfers can take place without a branch instruction (see Gerson, Col.1 lines 27-30), thereby improving the speed at which bit operations can take place (see Gerson, Abstract). Because it is desirable to improve the speed of processing all operations, let alone bit operations, one of ordinary skill in the art would have found it obvious to modify the bit value transfer instruction of Weng to be a write bit transfer instruction so that speed of bit processing operations is increased due to bit transfers being allowed to happen without a corresponding branch instruction.

48. Claim 16 is nearly identical to claim 39, differing in its parent claim, but encompassing the same scope as claim 39. Therefore, claim 16 is rejected for the same reasons as claim 39.

49. Regarding claims 17 and 40, taking claim 40 as exemplary, Weng in view of Gerson has taught the processor according to claim 39, but has not explicitly taught wherein the first write bit value transfer instruction specifies a zero status bit position as the source bit position of the first memory location.

50. However, while the bit transfer operation of Gerson involves transferring a value to and from the carry status bit, Gerson also has taught that any bit, such as an overflow bit, in the status register (Gerson, 28 of Fig.1) could also be used as the bit to be transferred into or from (see Gerson, Col.2 lines 26-34). Official Notice is taken that along with carry and overflow bits, a status register generally has a zero bit representing if a recent comparison had a result with a value of zero. Because Gerson has taught that any status bit can be used as a source and destination of a bit transfer operation, and it is well known that a zero bit is included as a status bit, one of ordinary skill in the art would have found it obvious to include the zero bit in the status register as a possible destination of a bit transfer operation.

51. Claim 17 is nearly identical to claim 40, differing in its parent claim, but encompassing the same scope as claim 40. Therefore, claim 17 is rejected for the same reasons as claim 40.

52. Regarding claims 18 and 41, taking claim 41 as exemplary, Weng in view of Gerson has taught the processor according to claim 40, wherein the first write bit value transfer instruction specifies a register as the second data memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

53. Claim 18 is nearly identical to claim 41, differing in its parent claim, but encompassing the same scope as claim 41. Therefore, claim 18 is rejected for the same reasons as claim 41.

54. Regarding claims 19 and 42, taking claim 42 as exemplary, Weng in view of Gerson has taught the processor according to claim 40, wherein the first write bit value transfer instruction specifies an address in data memory as the second data memory location (see above paragraph 9, as well as Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

55. Claim 19 is nearly identical to claim 42, differing in its parent claim, but encompassing the same scope as claim 42. Therefore, claim 19 is rejected for the same reasons as claim 42.

56. Regarding claims 20 and 43, taking claim 43 as exemplary, Weng has taught the processor according to claim 38, but has not explicitly taught wherein the bit value transfer instruction is a second write bit value transfer instruction.

57. However, Gerson has taught a test bit copy instruction which transfers a test bit value from a carry status bit memory location to a memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26) so that test bit transfers can take place without a branch instruction (see Gerson, Col.1 lines 27-30), thereby improving the speed at which bit operations can take place (see Gerson, Abstract). Because it is desirable to improve the speed of processing all operations, let alone bit operations, one of ordinary skill in the art would have found it obvious to modify the bit value transfer instruction of Weng to be a test bit transfer instruction so that speed of bit processing operations is increased due to bit transfers being allowed to happen without a corresponding branch instruction.

58. Claim 20 is nearly identical to claim 43, differing in its parent claim, but encompassing the same scope as claim 43. Therefore, claim 20 is rejected for the same reasons as claim 43.

59. Regarding claims 21 and 44, taking claim 44 as exemplary, Weng in view of Gerson has taught the processor according to claim 43, wherein the second write bit value transfer instruction specifies a carry status bit position as the source bit position of the first memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

60. Claim 21 is nearly identical to claim 44, differing in its parent claim, but encompassing the same scope as claim 44. Therefore, claim 21 is rejected for the same reasons as claim 44.

61. Regarding claims 22 and 45, taking claim 45 as exemplary, Weng in view of Gerson has taught the processor according to claim 44, wherein the second write bit value transfer instruction specifies a register as the second data memory location (see Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

62. Claim 22 is nearly identical to claim 45, differing in its parent claim, but encompassing the same scope as claim 45. Therefore, claim 22 is rejected for the same reasons as claim 45.

63. Regarding claims 23 and 46, taking claim 46 as exemplary, Weng in view of Gerson has taught the processor according to claim 44, wherein the second write bit value transfer instruction specifies an address in data memory as the second data memory location (see above paragraph 9, as well as Gerson, Col.2 lines 15-58 and Col.3 lines 6-26).

64. Claim 23 is nearly identical to claim 46, differing in its parent claim, but encompassing the same scope as claim 46. Therefore, claim 23 is rejected for the same reasons as claim 46.

Conclusion

65. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

66. Harriman, U.S. Patent No. 6,061,783, has taught a method for manipulating individual bits of memory operands without copying those operands into temporary registers.

67. James et al., U.S. Patent No. 6,523,108, has taught a method of extracting and transferring single bits from operands and specifying a source, destination, and the bit desired to be extracted.

68. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

69. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
4/27/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100